UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/694,574	10/24/2000	Young Jin Oh	8733.007.01	2428

30827 7590 04/14/2003

MCKENNA LONG & ALDRIDGE LLP
1900 K STREET, NW
WASHINGTON, DC 20006

EXAMINER
QI, ZHI QIANG

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 04/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Applicati n N .	Applicant(s)	
	09/694,574	OH ET AL.	
	Examiner	Art Unit	
	Mike Qi	2871	

-- Th MAILING DATE of this communication appears on the c ver sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *42-69* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *42-69* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/079,895* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 42-69 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-41 of U.S. Patent No. 6,281,957 in view of US 6,040,886 (Ota et al).

Claims 42-69, especially claims 42 and 56, of this application have corresponding limitations with the claims 1-41, especially the claims 1, 14, 28 and 41, of the US 6,281,957 except a few wording are different, and a limitation such as "a transparent first metal layer and a transparent second metal layer directly on the gate insulator" and a limitation such as "a transparent first metal layer including a plurality of first electrodes and a transparent second metal layer including a plurality of second electrodes on the gate insulator" are different, and that would be substantially obviousness-type double limitations.

Further, the reference US 6,040,886 (Ota et al) discloses (col.6, line 33- col.8, line 38; Fig.1) that the pixel electrode (3) (first metal layer) and the common electrode (5) (second metal layer) are formed on (also directly on the gate insulator, see Fig.1) the same layer and the same process as those signal electrodes (2,18), so that would simplify the manufacture process.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to arrange the pixel electrode and the common electrode directly on the gate insulator as claimed in this application for achieving simplify the manufacture process.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 42-52, 54-55 and 56-66, 68-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,852,485 (Shimada et al) in view of US 6,040,886 (Ota et al).

Claims 42 and 56, Shimada disclose (col.11 line 1 – col. 12, line 63; Figs.1-3) that an in-plane switching liquid crystal device comprising:

- active-matrix substrate (128) and counter substrate (127), i.e., first and second substrates;

- a plurality of gate bus lines (13) and source bus lines (14) (acting as data bus lines) on the first substrate (128), the gate lines (13) being crossed with the data bus lines (14);
- a common line (125) parallel to the gate lines (13) on the first substrate (128);
- a gate insulation layer (115) on the fist substrate lower plate (120);
- the picture element electrode (12, 16) and the counter electrode (11) are formed of conductive material, e.g., ITO transparent conductive material.

Shimada does not disclose the first metal layer (such as the pixel electrode) and the second metal layer (such as the common electrode) directly on the gate insulator.

However, Ota discloses (col.6, line 33 – col.8, line 38; Fig.1) that the pixel electrode (3) and the common electrode (5) are formed on the gate insulation film (7), and is directly on the insulator (7). Even though the pixel electrode (3) is serving as a source electrode or a drain electrode, but the function is a pixel electrode (3) to form the electric field E applied in the horizontal direction with the common electrode (5) so as to control the orientation of the liquid crystal molecules in the liquid crystal layer (see col.6, line 65 – col.7, line 6). Because the pixel electrode and the common electrode are formed on the same layer and the same process as those signal electrodes (2,18), so that would simplify the manufacture process.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to arrange the pixel electrode and the common electrode directly on the gate insulator as claimed in claims 42 and 56 for achieving simplify manufacture process.

Claims 43-44 and 57-58, Shimada disclose (col. 11, line 15 – col.12, line21, Figs.1-3) that a TFT (122) is at each of the intersections of the gate lines (13) and the source lines (14), i.e., a plurality of thin film transistors at crossing points of the gate bus lines and the data bus lines, and the TFT (122) includes a gate electrode (15) on the first substrate lower plate (120), a semiconductor layer (114) on the gate electrode (15), source electrodes (111) and drain electrodes (112) on the semiconductor layer (114).

Claims 45-46 and 59-60, Shimada disclose (col.11, lines 31-53; Figs.1-3) that the drain electrode (112) is connected to the picture element electrode (12 as the transparent first metal layer) through a connecting electrode (16) and a contact hole (17), the source electrode (111) is connected to the source line (14 as data line), and each counter electrode (as the second transparent metal layer) is connected to the common line through contact hole (col. 4, lines 23-26), i.e., the transparent second metal layer is connected to the common line.

Claims 47-48 and 61-62, Shimada disclose (col. 11, lines 32-53; Figs.1-3) that the connecting electrode (16) is connected to the picture element electrode (12), so that the electrode (16) also functions as pixel electrode, and the part of the electrode (16) overlapping the common line to form a storage capacitor. The part of the electrode (16) also overlapping the counter electrode (11) (Fig.3), so that forming another storage capacitor

Claims 49-50 and 63-64, Shimada disclose (col.12, lines 58-63; Figs.1-3) that the picture element electrode (12, 16) and the counter electrode (11) are formed of conductive material, e.g., ITO transparent conductive material, i.e., a transparent first

metal layer (data electrode or pixel electrode) and a transparent second metal layer (counter electrode or common electrode).

Claims 51-52, 54-55 and 65-66,68-69, Shimada disclose (col.13, line 66 – col. 14, line 9; Figs 1-3) that a first alignment layer (116) on the first substrate (128) and the second alignment layer (117) on the second substrate (127), and the material for the alignment layer is polyimide.

5. Claims 53 and 67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada and Ota as applied to claims 42-52, 54-55 and 56-66, 68-69 above, and further in view of US 5,929,958 (Ohta et al).

Claims 53 and 67, Ohta discloses (col.19, lines 26-39, col.20, lines 26-37; Fig.7) that an in-plane liquid crystal display device comprising a black matrix (BM) layer on the second substrate (SUB2), a color filter (FIL) on the black matrix layer (BM) and a liquid crystal layer (LC) between the first and second substrates (SUB1, SUB2), such that to improve the contrast and to prevent external light goes to the semiconductor layer (AS) of the TFT, so that protecting the TFT, and using color filter to display color signal.

Therefore, it would have been obvious to those skilled in the art at time the invention was made to arrange the black matrix, color filters as claimed in claims 53 and 67 for improving the contrast and display color signal.

Response to Arguments

6. Applicant's arguments filed on Aug.26, 2002 have been fully considered but they are not persuasive.

Applicant's **only** arguments are as follows:

1) The references Shimada and Ota do not disclose the transparent first metal layer (pixel electrode) and the transparent second metal layer (counter electrode or common electrode) are directly on the gate insulator, and would not render obvious as claimed in claims 42 and 56.

2) The reference Ohta fail to cure the deficiencies of Shimada in view of Ota.

Examiner's responses to Applicant's **only** arguments are as follows:

1) Although Shimada does not disclose the first metal layer (such as the pixel electrode) and the second metal layer (such as the common electrode) directly on the gate insulator. However, Ota discloses (col.6, line 33 – col.8, line 38; Fig.1) that the pixel electrode (3) and the common electrode (5) are formed on the gate insulation film (7), and is directly on the insulator (7). Even though the pixel electrode (3) is serving as a source electrode or a drain electrode, but the function is a pixel electrode (3) to form the electric field E applied in the horizontal direction with the common electrode (5) so as to control the orientation of the liquid crystal molecules in the liquid crystal layer (see col.6, line 65 – col.7, line 6). Because the pixel electrode and the common electrode are formed on the same layer and the same process as those signal electrodes (2,18), so that would simplify the manufacture process, and that would be motivation. Therefore, it would have been obvious to those skilled in the art at the time the invention was made to arrange the pixel electrode and the common electrode directly on the gate insulator as claimed in claims 42 and 56 for achieving simplify manufacture process.

2) The reference Ohta is a secondary reference discloses (col.19, lines

26-39, col.20, lines 26-37; Fig.7) that an in-plane liquid crystal display device comprising a black matrix (BM) layer on the second substrate (SUB2), a color filter (FIL) on the black matrix layer (BM) and a liquid crystal layer (LC) between the first and second substrates (SUB1, SUB2), such that to improve the contrast and to prevent external light goes to the semiconductor layer (AS) of the TFT, so that protecting the TFT, and using color filter to display color signal. Therefore, it would have been obvious to those skilled in the art at time the invention was made to arrange the black matrix, color filters as claimed in claims 53 and 67 for improving the contrast and display color signal.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (703) 308-6213.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Mike Qi
April 4, 2003

T. Chowdhury
Primary Examiner
Technology Center 2800